SESSION 19 – Honolulu Suite	
Novel Device Concepts	

Thursday, June 17, 10:20 a.m. Chairpersons: M-R Lin, AMD N. Nagashima, Sony

## 19.1 — 10:20 a.m.

**5nm-Gate Nanowire FinFET,** F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li\*, J.-W. Lee\*, P. Chen\*, M.-S. Liang and C. Hu, TSMC, Hsin-Chu, Taiwan, ROC, \*National Nano Device Laboratories, Hsin-Chu, Taiwan, ROC

A new nanowire FinFET structure is developed for CMOS device scaling into the sub-10nm regime. Accumulation mode P-FET and inversion mode N-FET with 5 nm and 10nm physical gate length, respectively, are fabricated. N-FET gate delay (CV/I) of 0.22ps and P-FET gate delay of 0.48 ps with excellent subthreshold characteristics are achieved, both with very low off leakage current less than 10 nA/um. Nanowire FinFET device operation is also explored using 3-D full quantum mechanical simulation.

# 19.2 — 10:45 a.m.

Selectively-Formed High Mobility SiGe-on-Insulator pMOSFETs with Ge-rich Strained Surface Channels Using Local Condensation Technique, T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama and S.-I. Takagi\*, MIRAI-ASET, Kawasaki, Japan, \*MIRAI-AIST, Kawasaki, Japan

A new approach to selectively form strained SiGe-on-Insulator (SGOI) channel transistors with very high Ge fraction on an SOI substrate is demonstrated. This method consists of epitaxial growth of SiGe layer with low Ge fraction and local oxidation processes. The obtained SGOI- pMOSFET with a Ge fraction of 93% has exhibited mobility enhancement up to 10 times. The thickness scalability of the SGOI channels was also confirmed down to 5 nm.

#### 19.3 — 11:10 a.m.

A Novel Sub-50 nm <u>Multi-Bridge-Channel MOSFET</u> (MBCFET) with Extremely High Performance, S.-Y. Lee, E.-J. Yoon, S.-M. Kim, C.W. Oh, M. Li, J.-D. Choi, K.-H. Yeo, M.-S. Kim, H.-J. Cho, S.-H. Kim, D.-W. Kim, D. Park and K. Kim, Samsung Electronics Co., Kyungki-Do, Korea

We demonstrate highly manufacturable sub-50 nm MBCFET with the Ion of 4.26mA/micrometer at VDD = 1.2V, which is the best performance ever reported. The excellent performance of MBCFET is resulted from the vertically stacked channels and the enhanced mobility. It has been fabricated on bulk Si substrate by using epitaxial growth of SiGe/Si/SiGe/Si layers and damascene gate process. It has structural and electrical merits in scaling and process integration.

### 19.4 — 11:35 a.m.

High Velocity Electron Injection MOSFETs for Ballistic Transistors using SiGe/Strained-Si Heterojunction Source Structures, T. Mizuno, N. Sugiyama, T. Tezuka, Y. Moriyama, S. Nakaharai, \*T. Maeda and \*S. Takagi, MIRAI-ASET, Kawasaki, Japan, \*MIRAI-AIST, Kawasaki, Japan

We have newly developed a high-velocity electron injection MOSFET for a ballistic transistor. Using the relaxed-SiGesource/strained-Si-channel heterostructures (hetero-MOSFETs), we have experimentally demonstrated, for the first time, that the transconductance is enhanced by the higher velocity injection, compared to those of strained-SOIs and conventional SOIs. We have also shown that the transconductance of hetero-MOSFETs strongly depends on the drain bias, because of the source heterojunction barriers.

## 19.5 — 12:00 p.m.

**Channel Design and Mobility Enhancement in Strained Germanium Buried Channel MOSFETs, H.** Shang, J.O. Chu, X. Wang\*, P.M. Mooney, K. Lee, J. Ott, K. Rim, K. Chan, K. Guarini and M. Ieong\*, IBM SRDC, Yorktown Heights, NY, \*IBM, Hopewell Junction, NY

The channel design space for scaled strained-Ge buried channel MOSFETs is examined by simulations and experiments. The identified Ge channel layer structure is scalable to sub-30nm devices. Strained-Ge buried-channel MOSFETs with an ultra-thin (1.5nm) Si cap are demonstrated with 6X hole mobility enhancement over the Si universal mobility. Compared with surface channel GeMOSFETs, buried strained-Ge channel structures can be integrated with fewer processing challenges to achieve a significantly enhanced hole mobility and an improved electron mobility.